software programmed to adjust the storage contents of the computer to reestablish in the context of the destination instruction a context logically equivalent to the context of the computer at the time of the control transfer instruction, the adjustment being determined, at least in part, by a classification of the control-transfer instruction; and

invoking circuitry to invoke the software before executing the destination instruction of at least some of the control transfer instructions.

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24. (once amended) A microprocessor, comprising:

an instruction pipeline designed to execute instructions of an instruction set, the instructions of the instruction set being classified into a relatively small number of classes relative to the number of instruction opcodes executable by the instruction pipeline, most divisions in the classification being based on a static encoding of instructions executed, with at most minor divisions in the classification being based on dynamic or data-dependent execution behavior;

a storage register designed to store, and circuitry designed to record without software intervention into the storage register, a value reflecting the class, from among the encoding-based classification, of an instruction recently executed by the pipeline.

REMARKS

The application was initially filed July 7, 1999, and a first Preliminary Amendment was filed December 15, 2000. This is a second Preliminary Amendment.

The Form 1449 filed herewith is cumulative of all previous 1449's, and adds several new references that have come to light since the previous IDS and Form 1449 were filed in December 2000. It is submitted that the claims distinguish all of these references, both before and after this amendment.

Claims 1 and 24 are now amended to clarify that the "class" stored in the second paragraphs of claims 1 and 24 is a class drawn from the classification scheme recited in the first paragraphs of these two claims. Because this was the only "class" recited in the claim before amendment, this limitation was inherent in claims 1 and 24 before the amendment. Thus, as in

Bose Corp. v. JBL Inc., 274 F.3d 1354, 1359-60, 61 USPQ2d 1216, 1218-19 (Fed. Cir. 2001), the amendment merely makes explicit what was previously implicit, and has no effect on the scope of the claims.

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. Kindly charge any additional fee, or credit any surplus, to Deposit Account 50-0675, Order No. 5231.4-4002.

Respectfully submitted,

SCHULTE ROTH & ZABEL

Dated: October 29, 2002

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REWRITTEN CLAIMS MARKED UP TO SHOW CHANGES

1. (once amended) A microprocessor and support software, comprising:

an instruction pipeline designed to execute instructions of an instruction set, control-transfer instructions of the instructions being instructions defined to transfer execution control of a computer from a source instruction to a destination instruction, control-flow instructions of the instruction set being classified into a relatively small plurality of classes relative to the number of instruction opcodes executable by the instruction pipeline, most divisions in the classification being based on a static encoding of control-flow instructions executed, with at most minor divisions in the classification being based on dynamic or data-dependent execution behavior;

a storage register designed to store, and updating circuitry active during execution of a program on the microprocessor, designed to record into the storage register, as part of the execution of control-flow instructions of the instruction set and without software intervention, a value reflecting the class, from among the encoding-based classification, of a control-flow instruction recently executed by the pipeline;

software programmed to adjust the storage contents of the computer to reestablish in the context of the destination instruction a context logically equivalent to the context of the computer at the time of the control transfer instruction, the adjustment being determined, at least in part, by a classification of the control-transfer instruction; and

invoking circuitry to invoke the software before executing the destination instruction of at least some of the control transfer instructions.

24. (once amended) A microprocessor, comprising:

an instruction pipeline designed to execute instructions of an instruction set, the instructions of the instruction set being classified into a relatively small number of classes relative to the number of instruction opcodes executable by the instruction pipeline, most divisions in the classification being based on a static encoding of instructions executed, with at most minor divisions in the classification being based on dynamic or data-dependent execution behavior;

a storage register designed to store, and circuitry designed to record without software intervention into the storage register, a value reflecting the class, from among the encoding-based classification, of an instruction recently executed by the pipeline.